DØ RunIIb Trigger Upgrade

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L1 Upgrades

- ➢ Central Track Trigger (L1CTT)
- ➢ Calorimeter Trigger (L1Cal)
- ➢ Calorimeter Track Match (L1CalTrack)

L2 Upgrades

- ➢ Silicon Track Trigger (L2STT)
- ➢ L2β Processors

L1 Tracking Trigger Upgrade

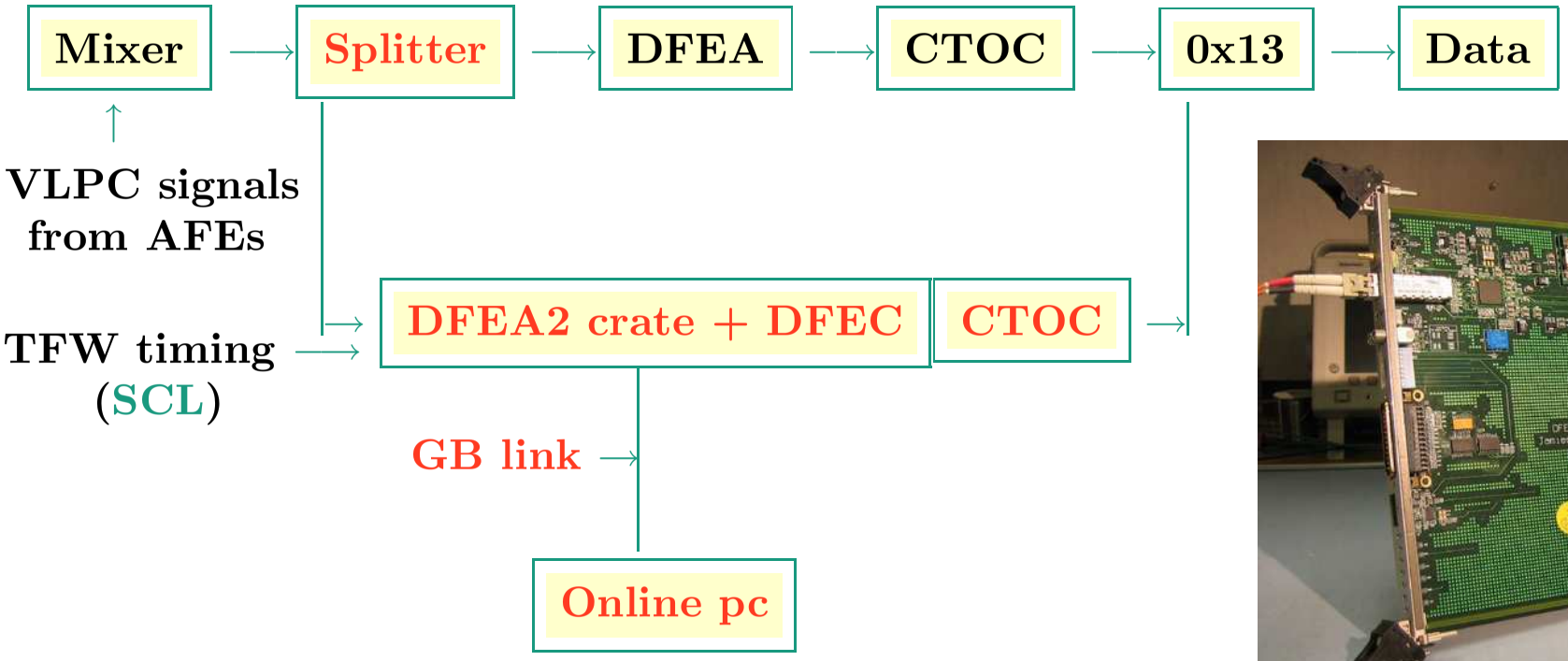
Motivation

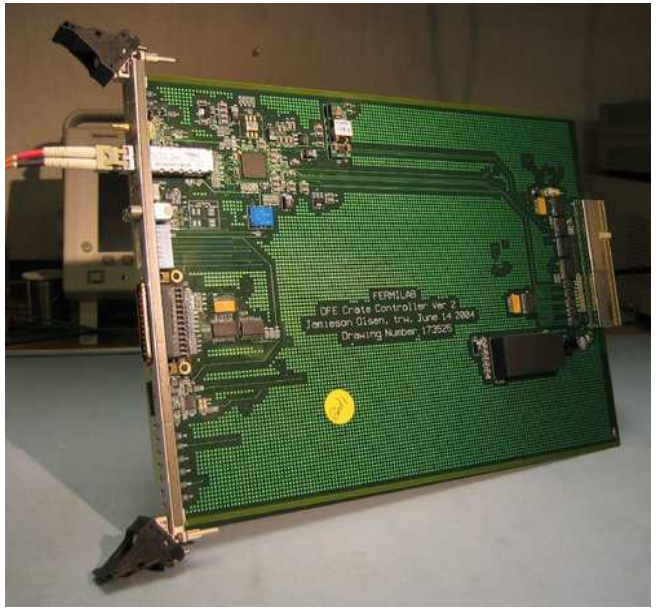
- Increase in luminosity → rate for fake tracks goes up as tracker occupancy grows
- Need to treat CFT axial layers as singlets rather than doublets in L1 trigger → 10x improvement in fake rejection rate at high p_T
- Larger FPGAs → major increase in the number of equations and number of terms per equation

New system improvements

- Very fast download through GB ethernet connection ≈ 10 min, compared to 24 hours now
- New boards have buffers - easy to check input/output data
- New controller (DFEC) gets the 53 MHz clock and controll bits from SCL and sends to DFEA2s → no more AFE dependence

Upgrade L1CTT Parallel Chain



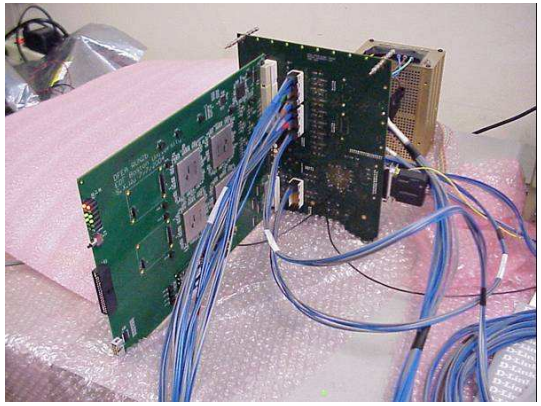


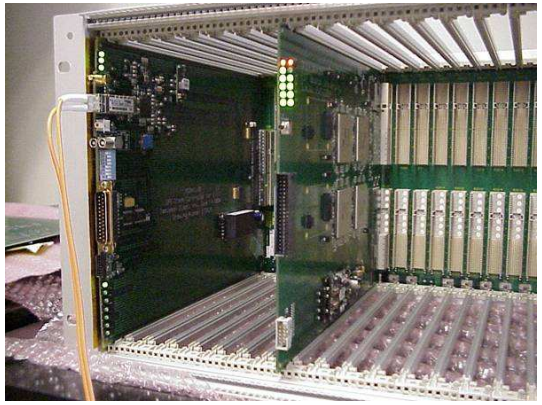
☞ Installation of prototype crate, two DFEA2 boards = 4 CTT sectors and DFEC in December 2004

☞ Run in parallel with existing CTT system without problems

L1CTT Comissioning

- 2 DFEA2 boards + DFEC on platform
- Firmware tests done in the CTT test stand
- Input signals go through LVDS splitters to DFEA/DFEA2
- Cable or board swapping require access to platform





✧ Parallel chain running allows us to:

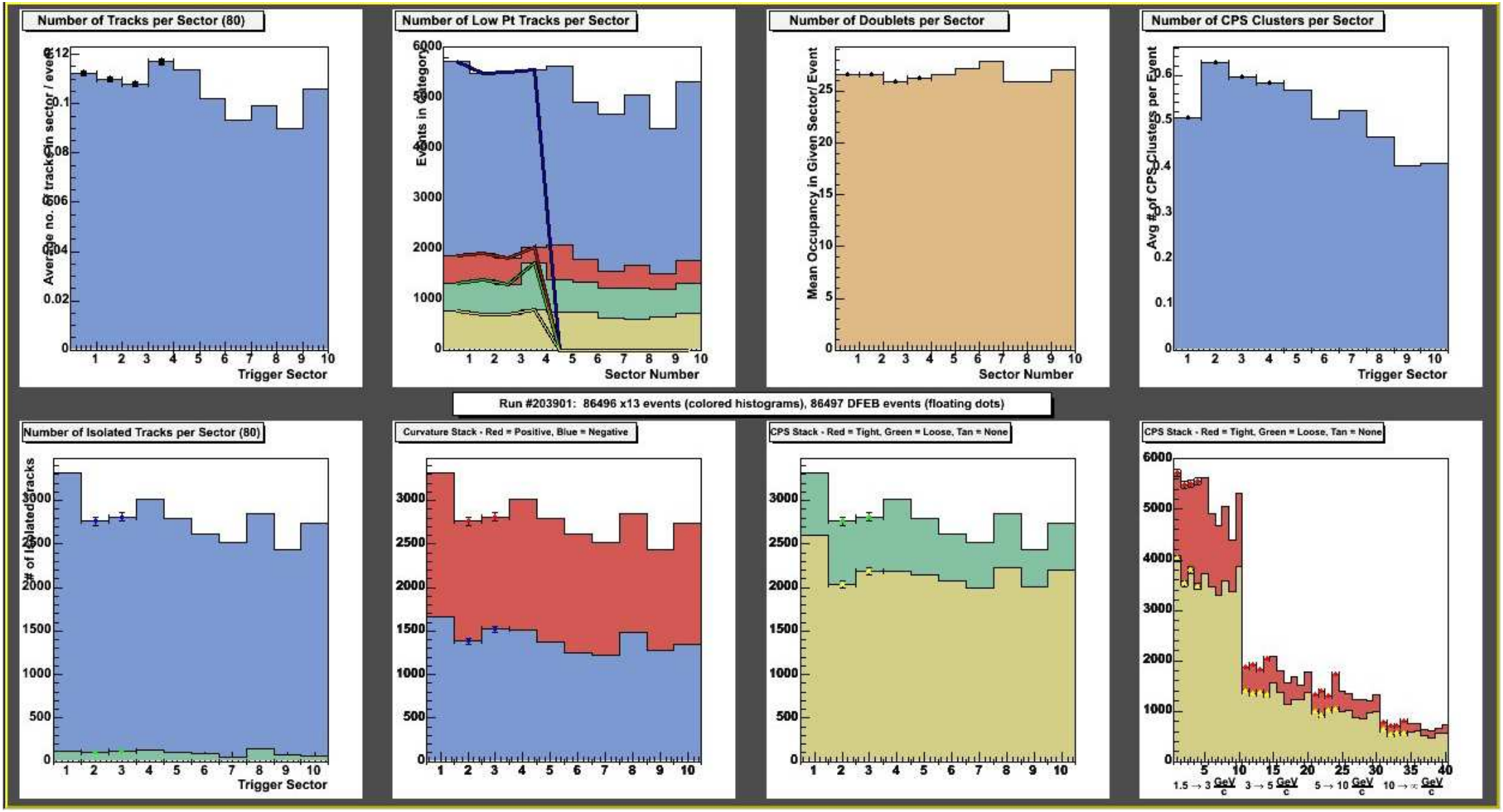
- test new system's hardware issues
- test software: downloading, diagnostics
- verify if new system (same equations; dead fibers turned off) produces similar results
- test efficiencies and rate using real data instead of simulation

DFEA2 Results and Future

- DFEA2 have been initalized and taking data without problems for around 3 months
- New system shows perfect agreement between the embedded control bits coming from the AFE, MIXER and the SCL
- DFEA2 happy with inputs and generates properly formatted output records
- Fake track test pattern with known input sent to DFEA2 → perfect output agreement
- Sectors having neighbouring information agree 100%
- Simulation and outputs from DFEA2 agree well for sector 0
- Boards being produced and arriving at Fermilab in May

DFEA2 runs very well

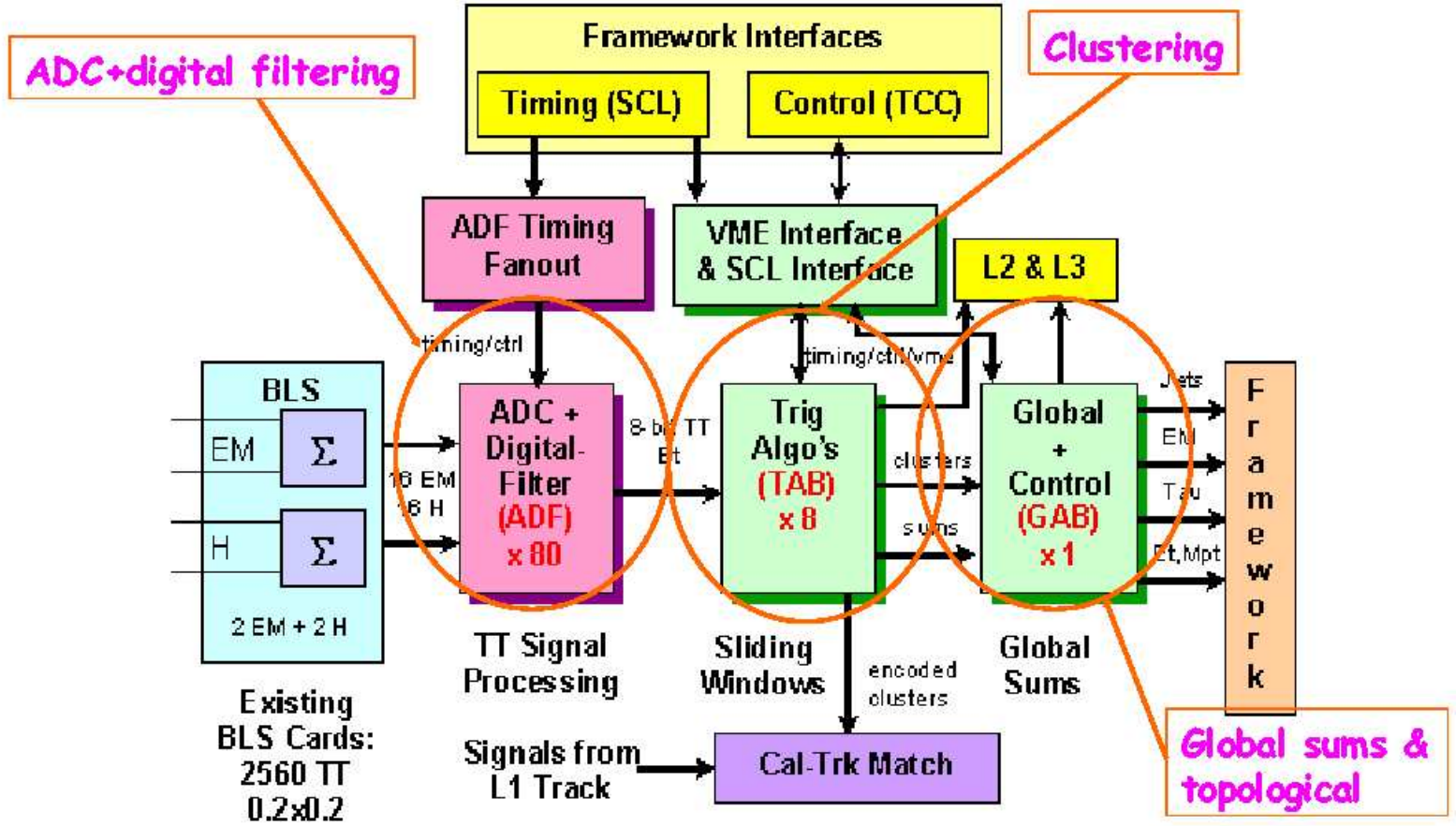
DFEA/DFEA2 Comparison



L1 Calorimeter Trigger Upgrade

Motivation

- Fixed size TT smaller than size of jets → slow turn-on curves for jet triggers → lots of low energetic jets passing at high luminosity
- Need topological triggers for different physics final states



L1Cal Trigger Upgrade Status

✧ TABs and GAB

- Production finished in December 2004
- Bench testing finished in January 2005 → no problems found
- Currently finishing up algorithm firmware
- Note: "structural" firmware already complete

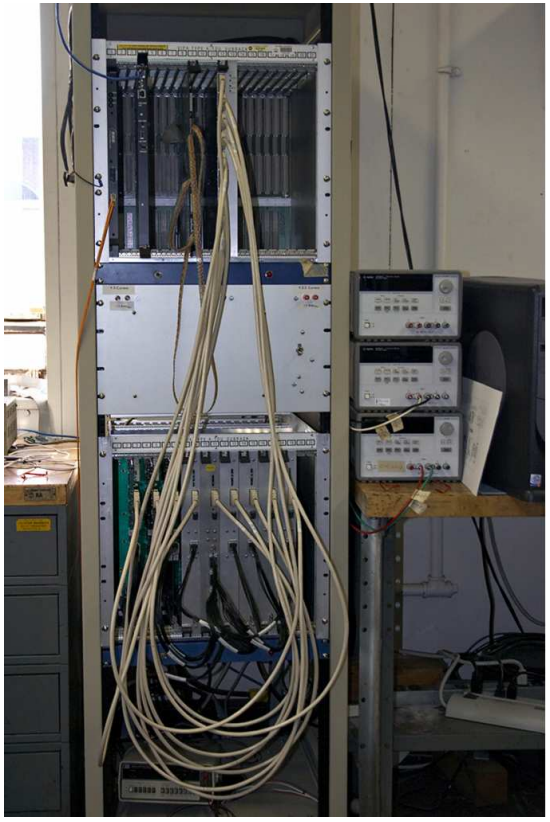
✧ ADF

- Prototype ADF v2's successfully bench tested
- PRR for ADF: 11 February → no issues identified
- First boards from production should have arrived at MSU
- All production boards expected March 8 → gain of over a month over current schedule

✧ BLS-to-ADF interface system

- Prototype design tested for noise performance in November → OK
- Some modifications considered to simplify cabling mechanics
- In review by engineers now

L1Cal Trigger Upgrade Status contd.



✧ Test system

- New Test System Manager: Mike Mulhearn
- Next round of integration tests to begin next week
- Hope to have a "vertical slice" test in $\sim$ 1 month

★ Vertical Slice = split TT signals $\rightarrow$ TAB $\rightarrow$ GAB $\rightarrow$ TFW

- data from TAB and GAB to tape

- More details about pre-installation work to come very soon

✧ Installation

- Coordinators: Linda Bagby & Dan Edmunds
- Physics Commissiong Coordinators: Sabine Lammers & Alan Stone
- All L1Cal hardware expected at Fermilab in July
- Schedule tuned to minimize experiment down-time

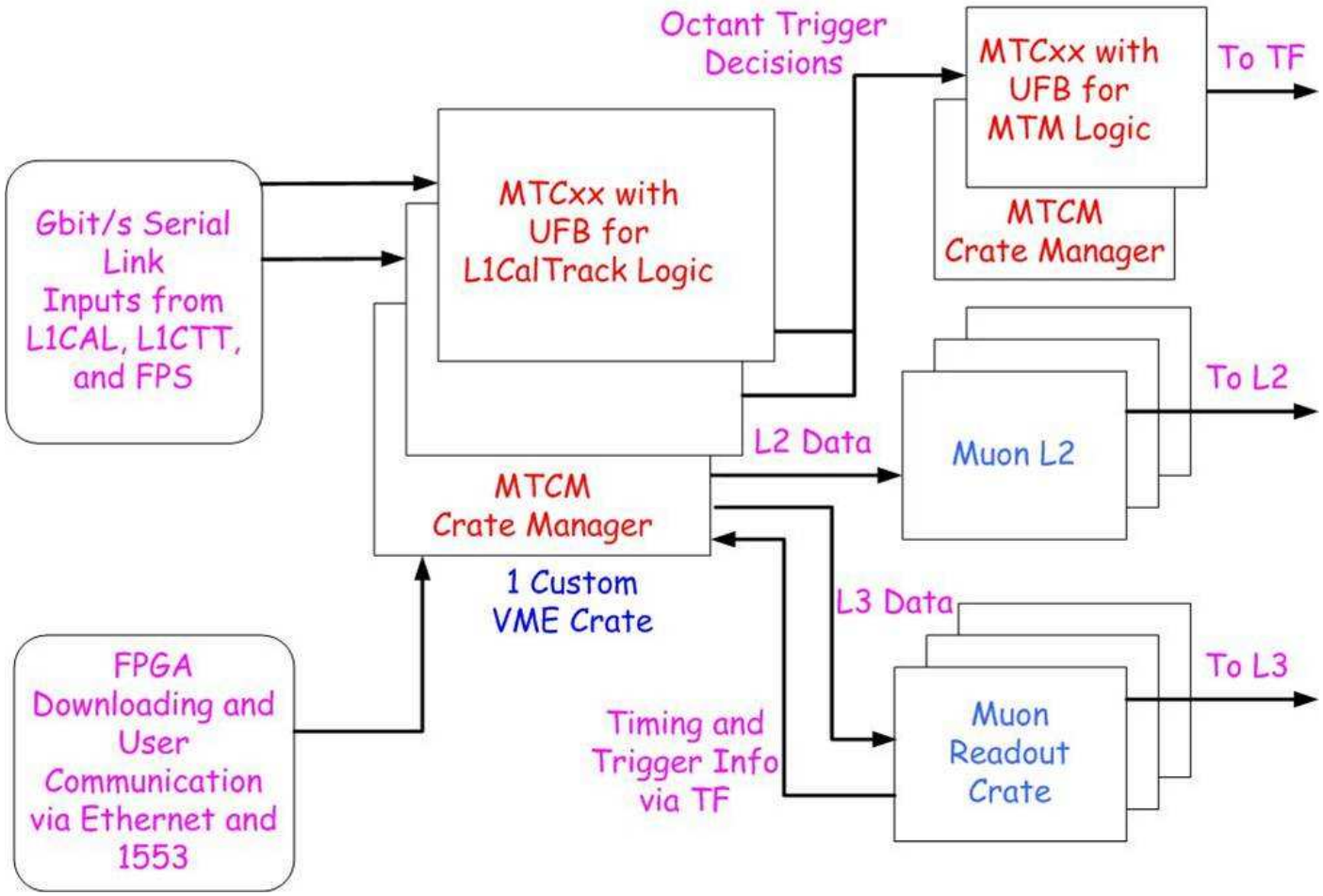
L1CalTrack Trigger Upgrade

Motivation

- Exploit L1Cal and L1CTT trigger upgrades to reduce combinatoric contributions to L1 trigger rate
- Trigger algorithms match ϕ position of EM/jet objects L1Cal with L1CTT
  - matching in E_T/p_T also available
  - isolation and CPS/FPS information also available
- Useful for any physics with high p_T electron or tau signatures
- Old simulation results show
  - EM rejection improved by a factor of $\sim$2
  - Fake rejection improved by a factor of $\sim$10

Use existing L1Mu-track architecture with small modifications

L1CalTrack Trigger System

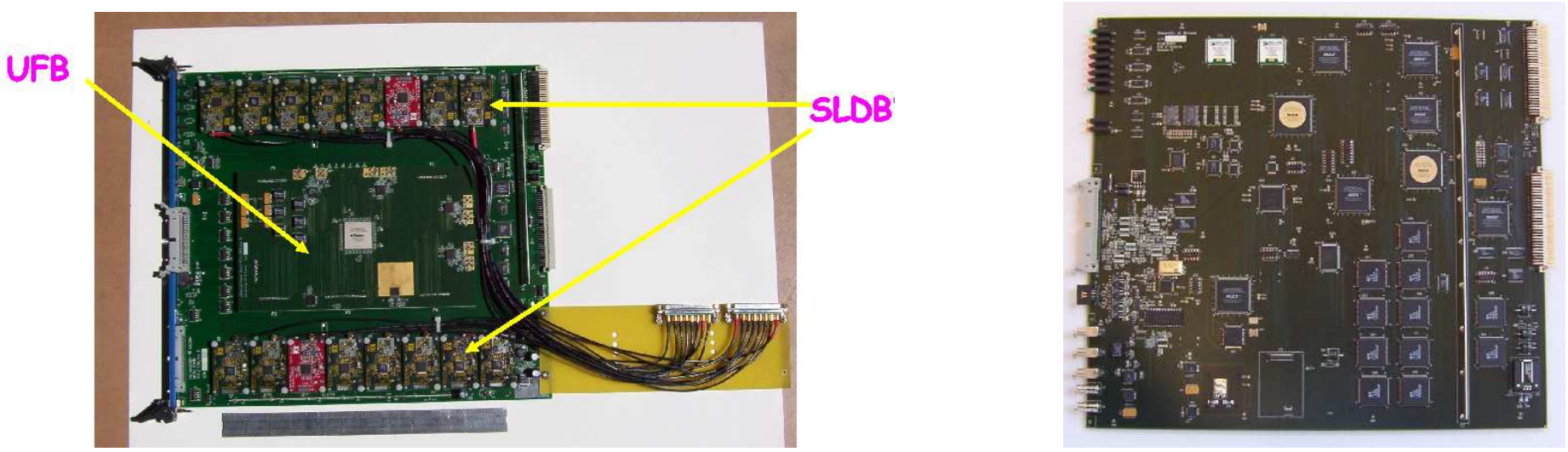


L1CalTrack Trigger Upgrade

Hardware status

- Crate manager (MTCM) production complete and testing in progress
- Trigger cards (MTCxx) in hand and bench testing underway
- Flavour boards (UBF) production assembled by Feb 11
- Splitter cards will be produced this spring

All major L1ClTrack cards in hand



MTCxx trigger card and MTCM Crate Manager

L1CalTrack Trigger Upgrade

Commissioning status

✧ Established L3 readout and L1 trigger capabilities of L1CalTrack crate using spare L1Mu cards

Work in progress

- Replace L1Mu MTCM with L1CalTrack MTCM beginning this week
- Replace L1Mu trigger cards with L1CalTrack trigger cards later this spring

✧ Once crates fully populated with L1CalTrack cards readout during collider running on a semi-regular basis

L2 Silicon Track Trigger Upgrade

Motivation

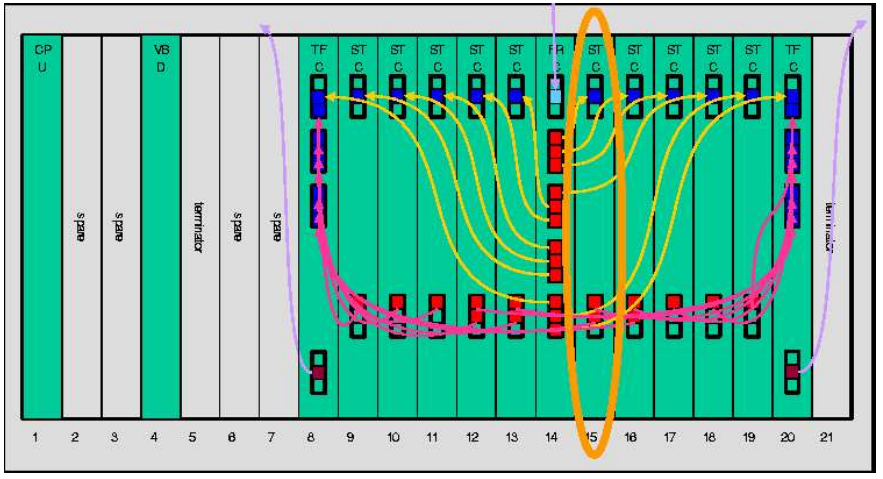
✧ Future SMT will consist of more sensors because of the inclusion of layer 0 (to compensate for dead ladders), thus L2 STT needs to be upgraded to cope with the extra inputs

Upgrade Decision:

- only one additional STC module per crate
- 30 more Buffer Controllers - production underway

✧ Hardware already in hand as spares from RunIIa

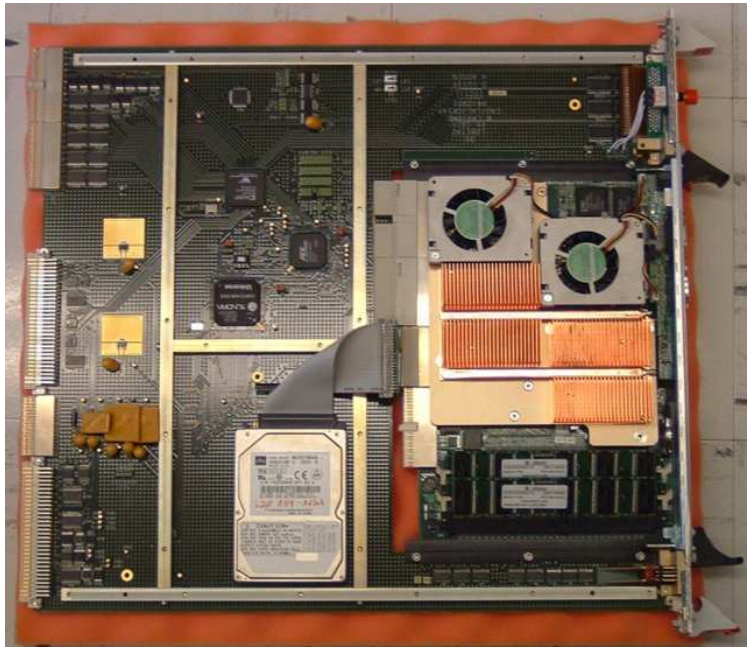
✧ Readout tests ongoing



RunIIb Crate layout

L2 β Processors Upgrade

- **Motivation:** Needed for more complex algorithms
- New processors could be installed at any time with minimal interruption
- "Drop-in" replacement of Single Board Computers in L2 system
- New SBC from Adlink-tech tested and met requirements (after resolving pci, power & manufacturer-specific I/O issues)
- Board provides dual P4 Xeons @ 2.4 GHz (current boards are Dual P3 @ 1GHz)
- Factor of two faster w/2.4GHz chips, compatible with future CPU in low-voltage Xeon line
- One 9u board modified & stress-tested for more than 2 weeks with fake data and L2 executable
- New processors ready in May 2005
- Testing of new cards to start at DAB this spring



Conclusions

- All trigger elements have entered production
- Next few months busy with testing and production
- Center of activity is moving to DAB
- There is a need for new people to get involved
- Very exciting times to come